UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,160	12/12/2001	Ken-Ming Li	21396-300101	9623

37509 7590 03/28/2005

DECHERT LLP
P.O. BOX 10004
PALO ALTO, CA 94303

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,160	LI ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40 and 44* is/are rejected.

7)☒ Claim(s) *41-43 and 45-56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-56 are pending in the instant application.

Claim Objections

2. Claims 1-56 objected to because of the following informalities:

Regarding claim 1, in line 3, "the associated delay" should be replaced by –the associated delays--, and, in line 4, "the input clock signal" should be replaced by –the input clock signals--.

Regarding claim 7, in line 2, "gates is coupled" should be replaced by –gates are coupled--.

Regarding claims 8 and 9, in line 1, "wherein one" should be replaced by –wherein a one--.

Regarding claim 13, in line 1, "the trigger signal" should be replaced by –the first trigger signal--.

Regarding claim 14, in line 2, "the first delay" is lacking antecedent basis.

Regarding claim 25, in line 2, "of an latest" should be replaced by –of a latest--.

Regarding claim 31, in lines 1-2, "derived from a reference clock" should be replaced by –according to a reference clock signal--.

Regarding claims 37 and 38, in lines 1-2, "the significant instant" should be replaced by –the delayed significant instant--.

Regarding claims 39, in line 2, "the significant instant" should be replaced by –the delayed significant instant--.

Regarding claims 40, in lines 1-2, "the significant instant" should be replaced by –the delayed significant instant--.

Regarding claim 46, in line 11, "the reference clock signal and" should be stricken, and, in line 15, "the synthesized" should be replaced by –the received—for limiting the claims to the proper embodiment of the invention.

Regarding claims 1-56, the use of the language "of a significant instant on a clock signal" in all claims is objected to. It is suggested by the Examiner that such phases are amended to be of the form --of a significant instant of a clock signal--. That is, the instants are "of" a signal rather than "on" a signal.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the claim is indefinite because "the input clock signal" in line 3 may not be definitely determined. A plurality of delay elements are defined. Further, each of the delay elements are defined as having an input configured to receive an input clock signal. Therefore, a plurality of input clock signals are defined respectively for the plurality of delay elements, and the determination of "the input clock signal" may not be made. That is, "the [*particular*] input clock signal" of *a particular* delay element

may not be distinguished among the plurality of input clock signals of the plurality of delay elements.

Regarding claims 2-5, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 6, the claim is indefinite because of the use of the language "each ... according to each" in line 2. Each gate corresponding to each delay does not provide a clear limitation. One is unable to determine exactly how the gates correspond to the delays.

Regarding claims 7-10, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 11, the claim is rejected for the same reasons as applied to claim 6 above.

Regarding claims 12-19, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 20, the claim is rejected for the same reasons as applied to claim 6 above.

Regarding claims 21-30, the claims are rejected as being based upon a rejected parent claim.

5. Claims 24-29, 34, 35, and 37-40 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. .

Regarding claims 24-29, the claims are rejected because, in each case, the base claim does not provide for more than one occurrence of the significant instant. The circuit as embodied and limited in claim 1 does not describe or provide for the detection of or response to more than one significant instant. The claim does not provide for the necessary structure and associated steps required to determine definitely the earliest or latest occurrence, a difference, an average, a median, or a standard deviation of a plurality of significant instants.

Regarding claims 34 and 35, the claims are rejected because, both cases, the base claim does not provide for more than one occurrence of the significant instant. The circuit as embodied and limited in claim 31 does not describe or provide for the detection of or response to more than one significant instant. The claim does not provide for the necessary structure and associated steps required to determine definitely the earliest or latest occurrence of a plurality of delayed significant instants.

Regarding claims 37-40, the claims are rejected because, each case, the base claim does not provide for the recording of a plurality of significant instants. The circuit as embodied and limited in claim 31 does not describe or provide for the detection of or response to more than one significant instant. The claim does not provide for the necessary structure and associated steps required to determine definitely the earliest or latest occurrence, a difference between an earliest and latest occurrence, or a statistic of the a plurality of delayed significant instants.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 6-12, 16, 18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubinec (US 5900834).

Regarding claim 1, Kubinec discloses by figure 3(a) an integrated circuit (col. 1, lines 54-59; col. 4, lines 58-65) with a jitter measurement or phase (Doppler) shift circuit (col. 3, lines 29-35), comprising: a plurality of delay elements (302a), each delay element having an associated delay (col. 6, lines 25-33; col. 7, lines 9-13), an input (DLYIN) configured to receive an input clock signal and an output (intermediate points between delay elements) responsive to the associated delay and the input clock signal, wherein the input clock signal has a significant instant or edge (col. 6, lines 33-39); a first set of circuitry (304) connected to the inputs and outputs of the plurality of delay elements, said first set of circuitry configured to detect the significant instant or edge on the input clock signal (col. 7, lines 23-35), the first set of circuitry further configured to output a signal (high voltage) responsive to the significant instant on the input clock signal (col. 7, lines 23-35); and a second set of circuitry (306) configured to receive the signal responsive to the significant instant on the input clock signal and a first trigger signal (MASTER CLOCK), the second set of circuitry further configured to latch or store the signal responsive to the significant instant on the input clock signal (col. 2, lines 9-

13; col. 3, lines 59-61), wherein a measure for jitter is determined from the latched signal responsive to the significant instant on the input clock signal (col. 3, lines 50-54). Kubinec discloses that the second set of circuitry counts the significant instants detected by the first set of circuitry. Therefore, the second set of circuitry stores the significant instants of the first set of circuitry. Kubinec does not explicitly disclose that the second set of circuitry stores the significant instants of the first set of circuitry responsive to a significant instant on the first trigger signal. However, it is apparent to one having ordinary skill in the art that the first trigger signal of Kubinec (fig. 3a, ref. "MASTER CLOCK") is utilized to latch the significant instants found by the first set of circuitry as is commonly performed in the art. According to the illustration of Kubinec (fig 3a) wherein the counters receive the master clock signal and the brief disclosure of the counters (col. 2, lines 9-13; col. 3, lines 59-61), it is implied or at least obvious that the counters latch the significant instants according to the master clock.

Regarding claim 2, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the associated delay of each delay element is approximately equal or uniform (col. 7, lines 9-13).

Regarding claim 3, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the plurality of delay elements are serially connected together (fig. 3a, refs. 302a).

Regarding claim 4, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the associated delay of each element is controlled by a calibration signal (figs. 3(b) and 3(c); col. 7, lines 9-20). The calibration signal controls

the length of each delay element as illustrated and described. Further, it is inherent that the calibration signal is generated by circuitry or calibration circuitry. Therefore, Kubinec discloses calibration circuitry or a delay control circuit.

Regarding claim 6, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the first set of circuitry comprises a plurality of two input logic gates, each two input logic gate corresponding to a delay element (fig. 3(a) and figs 4(a-e)).

Regarding claim 7, Kubinec discloses the limitations of claim 6 as applied above. Further, Kubinec discloses that the inputs of the plurality of two-input logic gates are coupled to the input and the output of one of the plurality of delay elements (fig. 3(a)).

Regarding claim 8, Kubinec discloses the limitations of claim 7 as applied above. Further, Kubinec discloses that, in various embodiments, one of the inputs of the two input logic gates are inverting inputs (figs. 4(b-d)). That is, the inputs with the "bubbles" are inverted inputs. Therefore, Kubinec discloses that one of the inputs of each of the plurality of two-input logic gates is coupled by means of an inverter logic gate.

Regarding claim 9, Kubinec discloses the limitations of claim 7 as applied above. Further, Kubinec discloses that one of the inputs of each of the plurality of two-input logic gates is coupled by means of wired connection (figs. (4a-e)).

Regarding claim 10, Kubinec discloses the limitations of claim 6 as applied above. Further, Kubinec discloses that each of the plurality of two-input logic gates is capable of producing a signal responsive to the significant instant on the input clock signal (col. 7, lines 20-35).

Regarding claim 11, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses by figure 3(a) that the second set of circuitry includes a first plurality of latching circuits (fig. 3(a), ref. 306) as applied to claim 1 above wherein the first plurality of latching circuits corresponding the plurality of delay elements (fig. 3(a)).

Regarding claim 12, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec disclose that the input clock signal (fig. 2(a), "RECEIVE") is related to a reference clock signal (fig. 2(a), "TRANSMIT"). The input clock signal is related to the reference clock signal because the input clock signal is a reflected version of the reference clock signal.

Regarding claim 16, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the measure for jitter is filtered or averaged (fig. 2(b), col. 4, lines 15-20).

Regarding claim 18, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses that the latched signal responsive to the significant instant on the input clock signal is recorded for a first number of significant instants on the first trigger signal. As applied to claim 16 above, the significant instants are averaged as disclosed by Kubinec. Therefore, the significant instants are recorded and summed for averaging over, as broadly as claimed, a first number of significant instants (col. 4, lines 15-20).

Regarding claim 23, Kubinec discloses the limitations of claim 1 as applied above. Further, Kubinec discloses a result calculator configured to provide information collected from the measure of jitter (fig. 2(a), ref. 230).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubinec in view of Yoon et al (US 6304116; hereafter "Yoon").

Regarding claim 5, Kubinec discloses the limitations of claim 4 as applied above. Kubinec discloses that the plurality of delay elements have an adjustable delay for properly capturing the significant instant of the input signal (figure 3(c)). Kubinec does not explicitly disclose that the delay control circuit is a charge pump controlled delay lock loop. However, Yoon teaches by figure 4 an exemplary plurality of delay elements (d1-dn) wherein the delay of each individual element is varied according to a voltage (VCON) determined by a charge pump (ref. 45; col. 3, lines 10-23). One skilled in the art is familiar with voltage controlled delay lines and the benefit of accuracy they provide. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a charge pump controlled delay line as taught by Yoon in place of the plurality of delay elements of Kubinec because the individual delays of each of the delay elements could be more accurately chosen for the proper capture of the significant instant of the input signal.

9. Claims 13, 14, 31-33, 36, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubinec in view of Riedle et al (US 6795515).

Regarding claim 13, Kubinec discloses the limitations of claim 12 as applied above. Further, according to figure 2(a) of Kubinec, as understood by one having skill

in the art, the reference generator oscillator (200) produces the trigger signal "MASTER CLOCK" of figure 3(a) used to latch the output of the edge detectors into memory. The phase or jitter difference is measured between the latched edge of period detection logic (220) against the latched edge of period detection logic (222) by the Doppler shift detector (230). Kubinec does not explicitly disclose that the trigger signal is delayed from the reference clock signal by a second delay. However, Riedle teaches a method of capturing a significant instant of a signal. Figure 2 of Riedle illustrates an input "DATA IN" which is fed into a delay line 24 and latched into latches 26. Further, Riedle teaches that the input signal must be accurately sampled or latched at the correct time to capture the significant instant of the input signal (col. 3, lines 20-62). The processor (fig. 2, ref. 25) applies a programmable delay to the clock signal (4ns o_CLOCK) such that the latches capture the significant instant of the delay line. One skilled in the art would readily apply the teachings of Riedle to the method of Kubinec because the timing of the trigger signal should be such that the latches of both the detection logics (fig. 2(a), refs. 220 and 222) are latched at a time when the difference in significant instants may be compared. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a programmable delay on the reference signal of Kubinec to create the trigger signal as taught by Riedle because the appropriate timing of the trigger signal is needed to measure the jitter between the transmit and receive signals.

Regarding claim 14, Kubinec in view of Riedle disclose the limitations of claim 13 as applied above. Further, it would have been obvious to one having skill in the art that

the first predetermined delay of the trigger signal would be longer than delay of the first delay element for the utility of the jitter measurement circuit. The first predetermined delay must be longer than the delay of the first delay element for the capture of a significant instant.

Regarding claim 31, Kubinec discloses by figure 3(a) a method for measuring jitter or a phase difference of a significant instant or edge of a clock signal derived from a reference clock signal (col. 2, lines 1-45), comprising: receiving an input clock signal (DLYIN), wherein the input clock signal has a significant instant (col. 6, lines 33-39); delaying the input clock signal (302a) by a first delay to produce a delayed input clock signal and a delayed significant instant on the delayed input clock signal (col. 2, lines 3-9); receiving a trigger signal (MASTER CLOCK); detecting (304) the delayed significant instant on the delayed input clock signal (col. 7, lines 23-35); and producing a jitter or phase measurement signal responsive to the delayed significant instant on the delayed input clock signal and the trigger signal (col. 3, lines 50-54). The delay line (fig 3(a), ref. 302a) creates a delayed version of the input signal including a delayed version of the input signal significant instant. According to figure 2(a) of Kubinec, as understood by one having skill in the art, the reference generator oscillator (200) produces the trigger signal "MASTER CLOCK" of figure 3(a) used to latch the output of the edge detectors into memory. The phase or jitter difference is measured between the latched edge of period detection logic (220) against the latched edge of period detection logic (222) by the Doppler shift detector (230). Kubinec does not explicitly disclose that the trigger signal is delayed from the reference clock signal by a second delay. However,

Riedle teaches a method of capturing a significant instant of a signal. Figure 2 of Riedle illustrates an input "DATA IN" which is fed into a delay line 24 and latched into latches 26. Further, Riedle teaches that the input signal must be accurately sampled or latched at the correct time to capture the significant instant of the input signal (col. 3, lines 20-62). The processor (fig. 2, ref. 25) applies a programmable delay to the clock signal (4ns o_CLOCK) such that the latches capture the significant instant of the delay line. One skilled in the art would readily apply the teachings of Riedle to the method of Kubinec because the timing of the trigger signal should be such that the latches of both the detection logics (fig. 2(a), refs. 220 and 222) are latched at a time when the difference in significant instants may be compared. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a programmable delay on the reference signal of Kubinec to create the trigger signal as taught by Riedle because the appropriate timing of the trigger signal is needed to measure the jitter between the transmit and receive signals.

Regarding claim 32, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses deriving a jitter measure through a comparison of the jitter measurement signal to the first delay (col. 4, lines 35-55). The jitter measurement is made with the knowledge of the time delay of each of the delay elements as disclosed by Kubinec.

Regarding claim 33, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses that the measure for jitter is filtered or averaged (fig. 2(b), col. 4, lines 15-20).

Regarding claim 36, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses that the latched signal responsive to the significant instant on the input clock signal is recorded for a first number of significant instants on the first trigger signal for averaging (fig. 2(b), col. 4, lines 15-20). Therefore, the significant instants are recorded and summed for averaging over a plurality of trigger signals (col. 4, lines 15-20).

Regarding claim 44, Kubinec in view of Riedle disclose the limitations of claim 31 as applied above. Further, Kubinec discloses inputting the reference clock signal to a circuit to produce the input clock signal (col. 3, lines 29-31).

Allowable Subject Matter

10. The indication of allowable subject matter is made regarding claims 41-43, and 45-56.

11. The following is a statement of reasons for the indication of allowable subject matter:

The indication of allowable subject matter is made regarding claims 41-43 and 45-56 because the prior art of record does not disclose a jitter measurement apparatus or method wherein a delay line is used to capture an input signal edge upon a delayed latch trigger for the measurement of the jitter and further utilizing the jitter measurement to adjust the jitter measurement circuit adaptively.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to show the state of the art with respect to jitter measurement circuits and methods.

U.S. Pat. No. 5272729 to Bechade et al.

U.S. Pat. No. 5457719 to Guo et al.

U.S. Pat. No. 5761254 to Behrin.

U.S. Pat. No. 5272390 to Watson et al.

U.S. Pat. No. 4713621 to Nakamura et al.

U.S. Pat. No. 4443766 to Belton.

U.S. Pat. No. 5289135 to Hoshino et al.

U.S. Pat. No. 5708382 to Park.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The Applicant is invited to call the examiner before the submittal of the next correspondence to discuss the allowable subject matter in the case to expedite the prosecution of the case. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
March 11, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER